

CLAIM AMENDMENTS

1-29. (canceled)

30. (currently amended) An amplifier stage, comprising:

a current source;

a first differential transistor having a source, gate, and drain, wherein the source of the first differential transistor is coupled to the current source;

a second differential transistor having a source, gate, and drain, wherein the source of the second differential transistor is coupled to the current source;

~~a first output resistor having positive and negative ends, wherein the negative end of the first output resistor is coupled to the drain of the first differential transistor;~~

~~a second output resistor having positive and negative ends, wherein the negative end of the second output resistor is coupled to the drain of the second differential transistor;~~

~~a first shunt peaking inductor having positive and negative ends, wherein the negative end of the first shunt peaking inductor is coupled to the positive end of the first output resistor; and~~

~~a second shunt peaking inductor having positive and negative ends, wherein the negative end of the second shunt peaking inductor is coupled to the positive end of the second output resistor~~

a first miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the first miller capacitance cancellation capacitor is coupled to the drain of the second differential transistor, and wherein the negative end of the first miller capacitance cancellation capacitor is coupled to the gate of the first differential transistor; and

a second miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the second miller capacitance cancellation capacitor is coupled to the drain of the first differential transistor, and wherein the negative end of the second miller capacitance cancellation capacitor is coupled to the gate of the second differential transistor.

31. (currently amended) The amplifier stage of claim 30, further comprising:
~~a first miller capacitance cancellation capacitor having positive and negative ends,~~
~~wherein the positive end of the first miller capacitance cancellation capacitor is coupled~~
~~to the drain of the second differential transistor, and wherein the negative end of the first~~
~~miller capacitance cancellation capacitor is coupled to the gate of the first differential~~
~~transistor; and~~

~~a second miller capacitance cancellation capacitor having positive and negative~~
~~ends, wherein the positive end of the second miller capacitance cancellation capacitor is~~
~~coupled to the drain of the first differential transistor, and wherein the negative end of the~~
~~second miller capacitance cancellation capacitor is coupled to the gate of the second~~
~~differential transistor~~

a first output impedance having positive and negative ends, wherein the negative
end of the first output impedance is coupled to the drain of the first differential transistor;

a second output impedance having positive and negative ends, wherein the
negative end of the second output impedance is coupled to the drain of the second
differential transistor.

32. (previously presented) The amplifier stage of claim 30, wherein:
the current source comprises a current source transistor having a gate, source, and
drain; and
the gate of the current source transistor is coupled to a bias voltage.

33. (currently amended) The amplifier stage of claim 32, wherein:
the first and second differential transistors and the current source transistor
comprise NMOS transistors or PMOS transistors.

34. (currently amended) The amplifier stage of claim 30, further comprising
32, wherein:

~~the first and second differential transistors and the current source transistor~~
~~comprise PMOS transistors~~

a first output impedance having positive and negative ends, wherein the negative end of the first output impedance is coupled to the drain of the first differential transistor and the positive end of the first output impedance is coupled to a voltage supply; and

a second output impedance having positive and negative ends, wherein the negative end of the second output impedance is coupled to the drain of the second differential transistor and the positive end of the second output impedance is coupled to the voltage supply.

35. (previously presented) An amplifier stage, comprising:

- a current source;
- a first differential transistor having a source, gate, and drain, wherein the source of the first differential transistor is coupled to the current source;
- a second differential transistor having a source, gate, and drain, wherein the source of the second differential transistor is coupled to the current source;
- a first series peaking inductor having positive and negative ends, wherein the negative end of the first series peaking inductor is coupled to the gate of the first differential transistor;
- a second series peaking inductor having positive and negative ends, wherein the negative end of the second series peaking inductor is coupled to the gate of the second differential transistor;
- a first miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the first miller capacitance cancellation capacitor is coupled to the drain of the second differential transistor, and wherein the negative end of the first miller capacitance cancellation capacitor is coupled to the gate of the first differential transistor; and
- a second miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the second miller capacitance cancellation capacitor is coupled to the drain of the first differential transistor, and wherein the negative end of the second miller capacitance cancellation capacitor is coupled to the gate of the second differential transistor.

36. (previously presented) The amplifier stage of claim 35, wherein:

- the current source comprises a current source transistor having a gate, source, and drain; and
- the gate of the current source transistor is coupled to a bias voltage.

37. (previously presented) The amplifier stage of claim 36, wherein:

- the first and second differential transistors and the current source transistor comprise NMOS transistors.

38. (previously presented)The amplifier stage of claim 36, wherein:
the first and second differential transistors and the current source transistor
comprise PMOS transistors.

39. (previously presented) An amplifier stage, comprising:

a current source;

a first differential transistor having a source, gate, and drain, wherein the source of the first differential transistor is coupled to the current source;

a second differential transistor having a source, gate, and drain, wherein the source of the second differential transistor is coupled to the current source;

a first output resistor having positive and negative ends, wherein the negative end of the first output resistor is coupled to the drain of the first differential transistor;

a second output resistor having positive and negative ends, wherein the negative end of the second output resistor is coupled to the drain of the second differential transistor;

a first shunt peaking inductor having positive and negative ends, wherein the negative end of the first shunt peaking inductor is coupled to the positive end of the first output resistor;

a second shunt peaking inductor having positive and negative ends, wherein the negative end of the second shunt peaking inductor is coupled to the positive end of the second output resistor;

a first miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the first miller capacitance cancellation capacitor is coupled to the drain of the second differential transistor, and wherein the negative end of the first miller capacitance cancellation capacitor is coupled to the gate of the first differential transistor; and

a second miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the second miller capacitance cancellation capacitor is coupled to the drain of the first differential transistor, and wherein the negative end of the second miller capacitance cancellation capacitor is coupled to the gate of the second differential transistor.

40. (previously presented) The amplifier stage of claim 39, wherein:

the current source comprises a current source transistor having a gate, source, and drain; and

the gate of the current source transistor is coupled to a bias voltage.

41. (previously presented) The amplifier stage of claim 40, wherein:
the first and second differential transistors and the current source transistor
comprise NMOS transistors.

42. (previously presented) The amplifier stage of claim 40, wherein:
the first and second differential transistors and the current source transistor
comprise PMOS transistors.

43. (currently amended) A multi-stage differential amplifier, comprising:
 a first amplifier stage, that includes a first differential transistor having a first source, a first gate, and a first drain, and a second differential transistor having a second source, a second gate, and a second drain, having a positive signal input, a negative signal input, a positive signal output, and a negative signal output;

a second amplifier stage having a positive signal input, a negative signal input, a positive signal output, and a negative signal output;

wherein the positive signal output of the first amplifier stage is coupled to the positive signal input of the second amplifier stage, and wherein the negative signal output of the first amplifier stage is coupled to the negative signal input of the second amplifier stage;

wherein the first amplifier stage includes a first pair of series peaking inductors, a first pair of shunt peaking inductors, and a first pair of miller capacitance cancellation capacitors;

wherein a first miller capacitance cancellation capacitor, of the first pair of miller capacitance cancellation capacitors, having positive and negative ends, wherein the positive end of the first miller capacitance cancellation capacitor is coupled to the second drain of the second differential transistor, and wherein the negative end of the first miller capacitance cancellation capacitor is coupled to the first gate of the first differential transistor;

wherein a second miller capacitance cancellation capacitor, of the first pair of miller capacitance cancellation capacitors, having positive and negative ends, wherein the positive end of the second miller capacitance cancellation capacitor is coupled to the first drain of the first differential transistor, and wherein the negative end of the second miller capacitance cancellation capacitor is coupled to the second gate of the second differential transistor; and

wherein the second amplifier stage includes a second pair of series peaking inductors and a second pair of shunt peaking inductors.

44. (previously presented) The multi-stage differential amplifier of claim 43, further comprising:

a third amplifier stage having a positive signal input, a negative signal input, a positive signal output, and a negative signal output;

wherein the positive signal output of the second amplifier stage is coupled to the positive signal input of the third amplifier stage, and wherein the negative signal output of the second amplifier stage is coupled to the negative signal input of the third amplifier stage; and

wherein the third amplifier stage includes a third pair of series peaking inductors, a third pair of shunt peaking inductors, and a second pair of miller capacitance cancellation capacitors.

45. (previously presented) The multi-stage differential amplifier of claim 44, further comprising:

a fourth amplifier stage having a positive signal input, a negative signal input, a positive signal output, and a negative signal output;

wherein the positive signal output of the third amplifier stage is coupled to the positive signal input of the fourth amplifier stage, and wherein the negative signal output of the third amplifier stage is coupled to the negative signal input of the fourth amplifier stage; and

wherein the fourth amplifier stage includes a fourth pair of series peaking inductors and a third pair of miller capacitance cancellation capacitors.

46. (previously presented) The multi-stage differential amplifier of claim 45, further comprising:

a fifth amplifier stage having a positive signal input, a negative signal input, a positive signal output, and a negative signal output;

wherein the positive signal output of the fourth amplifier stage is coupled to the positive signal input of the fifth amplifier stage, and wherein the negative signal output of the fourth amplifier stage is coupled to the negative signal input of the fifth amplifier stage; and

wherein the fifth amplifier stage includes a fourth third pair of shunt peaking inductors.

47. (previously presented)The multi-stage differential amplifier of claim 46, further comprising:

a sixth amplifier stage having a positive signal input, a negative signal input, a positive signal output, and a negative signal output;

wherein the positive signal output of the fifth amplifier stage is coupled to the positive signal input of the sixth amplifier stage, and wherein the negative signal output of the fifth amplifier stage is coupled to the negative signal input of the sixth amplifier stage.

48. (previously presented)The multi-stage differential amplifier of claim 43, wherein:

each shunt peaking inductor of the first pair of shunt peaking inductors is coupled in series with a corresponding output resistor.

49. (previously presented)The multi-stage differential amplifier of claim 43, wherein:

each shunt peaking inductor of the second pair of shunt peaking inductors is coupled in series with a corresponding output resistor.

50. (previously presented)The multi-stage differential amplifier of claim 43, wherein:

at least one of the first amplifier stage and the second amplifier stage includes:

a current source;

a first differential transistor having a source, gate, and drain, wherein the source of the first differential transistor is coupled to the current source; and

a second differential transistor having a source, gate, and drain, wherein the source of the second differential transistor is coupled to the current source.

51. (previously presented)The multi-stage differential amplifier of claim 50, wherein:

the current source comprises a current source transistor having a gate, source, and drain; and

the gate of the current source transistor is coupled to a bias voltage.

52. (previously presented) The multi-stage differential amplifier of claim 51, wherein:

the first and second differential transistors and the current source transistor comprise NMOS transistors.

53. (previously presented) The multi-stage differential amplifier of claim 51, wherein:

the first and second differential transistors and the current source transistor comprise PMOS transistors.

54. (currently amended) A multi-stage differential amplifier, comprising:
 a first amplifier stage, that includes a first differential transistor having a first source, a first gate, and a first drain, and a second differential transistor having a second source, a second gate, and a second drain, having a positive signal input, a negative signal input, a positive signal output, and a negative signal output;

a second amplifier stage having a positive signal input, a negative signal input, a positive signal output, and a negative signal output;

wherein the positive signal output of the first amplifier stage is coupled to the positive signal input of the second amplifier stage, and wherein the negative signal output of the first amplifier stage is coupled to the negative signal input of the second amplifier stage;

wherein the first amplifier stage includes a first pair of series peaking inductors, a first pair of shunt peaking inductors, and a first pair of miller capacitance cancellation capacitors;

wherein a first miller capacitance cancellation capacitor, of the first pair of miller capacitance cancellation capacitors, having positive and negative ends, wherein the positive end of the first miller capacitance cancellation capacitor is coupled to the second drain of the second differential transistor, and wherein the negative end of the first miller capacitance cancellation capacitor is coupled to the first gate of the first differential transistor;

wherein a second miller capacitance cancellation capacitor, of the first pair of miller capacitance cancellation capacitors, having positive and negative ends, wherein the positive end of the second miller capacitance cancellation capacitor is coupled to the first drain of the first differential transistor, and wherein the negative end of the second miller capacitance cancellation capacitor is coupled to the second gate of the second differential transistor;

wherein each shunt peaking inductor of the first pair of shunt peaking inductors is coupled in series with a corresponding output resistor;

wherein the second amplifier stage includes a second pair of series peaking inductors and a second pair of shunt peaking inductors;

wherein each shunt peaking inductor of the second pair of shunt peaking inductors is coupled in series with a corresponding output resistor;

a third amplifier stage having a positive signal input, a negative signal input, a positive signal output, and a negative signal output;

wherein the positive signal output of the second amplifier stage is coupled to the positive signal input of the third amplifier stage, and wherein the negative signal output of the second amplifier stage is coupled to the negative signal input of the third amplifier stage;

wherein the third amplifier stage includes a third pair of series peaking inductors, a third pair of shunt peaking inductors, and a second pair of miller capacitance cancellation capacitors; and

wherein each shunt peaking inductor of the third pair of shunt peaking inductors is coupled in series with a corresponding output resistor.

55. (previously presented) The multi-stage differential amplifier of claim 54, wherein:

at least one of the first amplifier stage and the second amplifier stage includes:

a current source;

a first differential transistor having a source, gate, and drain, wherein the source of the first differential transistor is coupled to the current source; and

a second differential transistor having a source, gate, and drain, wherein the source of the second differential transistor is coupled to the current source.

56. (previously presented) The multi-stage differential amplifier of claim 55, wherein:

the current source comprises a current source transistor having a gate, source, and drain; and

the gate of the current source transistor is coupled to a bias voltage.

57. (previously presented) The multi-stage differential amplifier of claim 56, wherein:

the first and second differential transistors and the current source transistor comprise NMOS transistors.

58. (previously presented) The multi-stage differential amplifier of claim 56, wherein:

the first and second differential transistors and the current source transistor comprise PMOS transistors.